AMENDMENTS TO THE SPECIFICATION:

Please delete the abstract, at page 32 of the specification, and replace it with the attached new abstract. Also, please amend the specification as described below.

Please replace the paragraph beginning at page 3, line 6, with the following:

NPN transistors (NP11 to NP1n, NP21 to NP2n) having different emitter areas (in the present example, the ratio of the areas is N:1) are connected to two input terminals (+, -) of the differential amplifier OP1 ~~via diodes~~. Moreover, n NPN transistors are connected in series. Then, a potential difference ΔVBE occurs per stage, so that with the n NPN transistors, a potential difference nΔVBE occurs between [[the]] both ends of R1. If PMOS FETs (P61, P62) have an equal W (channel width)/L (channel length) size, an equal current flows through the respective series NPN bipolar transistors. A voltage VOUT is expressed as follows:

$$VOUT = \alpha n\Delta VBE + nVBE = n(\alpha\Delta VBE + VBE) \cong 1.2\ nV \quad (2)$$

If this output is reduced to 1/n, a voltage of 1.2 V is obtained as in the case with the circuit in FIG. 4. In this case, α is almost equal to the α in FIG. 4.

Please delete the paragraphs beginning at page 5, line 3, and ending at page 12, line 18, and add the following new paragraphs:

The present invention provides a constant voltage generating circuit comprising a plurality of first bipolar transistors, a number of the plurality of first bipolar transistors being n (an integer; $2 \leq n$), each of the plurality of first bipolar transistors having an emitter area, a plurality of second bipolar transistors including n second bipolar transistors each having an associated emitter area greater than the emitter area of each of the plurality of first bipolar transistors, differential voltage generating means for generating a differential voltage between a voltage equal to a sum of base emitter voltages of the n first bipolar transistors and a sum of base emitter voltages of the n second bipolar transistors, and voltage amplification adding means for amplifying the differential voltage and adding the amplified voltage to the base emitter voltage of one of the plurality of second bipolar transistors to output a constant voltage independent of temperature and substantially independent of the number of the plurality of first bipolar transistors and the number of the plurality of second bipolar transistors.

The present invention also provides a constant voltage generating circuit wherein the differential voltage generating means includes a differential amplifier, and an offset voltage at the differential amplifier in input equivalent has a primary temperature characteristic.

The present invention also provides a constant voltage generating circuit comprising a plurality of first bipolar transistors, a number of the plurality of first bipolar transistors being n (an integer; $2 \leq n$) , each of the plurality of first bipolar transistors

having an emitter area, a plurality of second bipolar transistors including n second bipolar transistors each having an associated emitter area greater than the emitter area of each of the plurality of the first bipolar transistors, differential voltage generating means for generating a differential voltage between a voltage equal to a sum of base emitter voltages of the n first bipolar transistors and a sum of base emitter voltages of the n second bipolar transistors, and voltage amplification adding means including a differential amplifier in which an offset voltage in input equivalent has a primary temperature characteristic, for amplifying the differential voltage and adding the amplified voltage to the sum of the base emitter voltages of the n second bipolar transistors to output a constant voltage independent of temperature and substantially independent of the number of the plurality of first bipolar transistors and the number of the plurality of second bipolar transistors.

The present invention also provides a constant voltage generating circuit comprising a plurality of first pnp transistors including n (an integer; $2 \leq n$) first pnp transistors, a collector of each of the plurality of first pnp transistors being grounded, a base of a one of the plurality of first pnp transistors being grounded, a base of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of first pnp transistors, a plurality of second pnp transistors including n second pnp transistors each having an emitter area greater than the first pnp transistors, a collector of each of the plurality of second pnp transistors being grounded, a base of a first one of the plurality of second pnp transistors being grounded, a collector of each of the plurality of second pnp transistors being grounded, a base of a k-th one of the plurality of second pnp transistors except for an another one

of the plurality of second pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of second pnp transistors, current sources connected to the respective emitters of the plurality of first pnp transistors and the respective emitters of the plurality of second pnp transistors, except for a emitter of the first one of the plurality of second pnp transistors to supply currents to the respective pnp transistors of the pluralities of first and second pnp transistors, two resistors being connected in series between the emitter of the first one of the of plurality of second pnp transistors and the corresponding current source, a connection point between the two resistors being connected to the base of the another one of the plurality of second pnp transistors, and current control means including a first input terminal to which the emitter of a n-th one of the plurality of first pnp transistors is connected and a second input terminal to which the emitter of a n-th one of the plurality of second pnp transistors is connected, the current control means controlling currents from the current sources by outputting a control signal that controls the currents from the current sources so that a potential at the first input terminal and a potential at the second input terminal are the same.

The present invention also provides a constant voltage generating circuit comprising a plurality of first npn transistors including n (an integer; $2 \leq n$) first npn transistors, a base and a collector of each of the plurality of first npn transistors being connected together, an emitter of a one of the plurality of first npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first npn transistors being connected to a collector of a (k-1)-th one of the plurality of first npn transistors, a plurality of second npn transistors including n second npn transistors each having an emitter area greater than each of the plurality of first npn transistors, a base

and a collector of each of the plurality of second npn transistors being connected together, an emitter of a one of the plurality of second npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of second npn transistors, except an another one of the plurality of second npn transistors being connected to a collector of a (k-1)-th one of the plurality of second npn transistors, current sources connected to the collector of a n-th one of the plurality of first npn transistors and the collector of a n-th one the plurality of second npn transistors to supply currents to the respective npn transistors of the pluralities of first and second npn transistors, the one of the plurality of second npn transistors being connected to the corresponding current source via two resistors connected in series, a connection point between the two resistors being connected to an emitter of the another one of the plurality of second npn transistors, and current control means including a first input terminal to which the collector of the n-th one of the plurality of first npn transistors is connected and a second input terminal to which the collector of the n-th one of the plurality of second npn transistors is connected, the current control means controlling currents from the current sources by outputting a control signal that controls the currents from the current sources so that a potential at the first input terminal and a potential at the second input terminal are the same.

The present invention also provides a constant voltage generating circuit further comprising a differential voltage generating means which includes a differential amplifier, and an offset voltage at the differential amplifier in input equivalent has a primary temperature characteristic.

The present invention also provides a constant voltage generating circuit comprising a plurality of first pnp transistors including n (an integer; $2 \leq n$) first pnp transistors, a collector of each of the plurality of first pnp transistors being grounded, a base of a one of the plurality of first pnp transistors being grounded, a base of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of first pnp transistors, a plurality of second pnp transistors including n second pnp transistors each having an emitter area greater than each of the plurality of first pnp transistors, a collector of each of the plurality of second pnp transistors being grounded, a base of a one of the plurality of second pnp transistors being grounded, a base of a k-th one of the plurality of second pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of second pnp transistors, current sources connected to the respective emitters of the plurality of first pnp transistors and the respective emitters of the plurality of second pnp transistors except an emitter of the n-th one of the plurality of second pnp transistors to supply currents to the respective pnp transistors of the pluralities of first and second pnp transistors, two resistors being connected in series between the emitter of the n-th one of the plurality second pnp transistors and the corresponding current source, and current control means including a first input terminal to which the emitter of a n-th one of the plurality of first pnp transistors is connected, a second input terminal to which a connection point between the two resistors connected in series is connected, and a differential amplifier, the current control means controlling currents from the current sources by outputting a control signal that controls the currents from the current sources so that a potential at the first input terminal and a potential at the second input terminal

are the same, an offset voltage at the differential amplifier in input equivalent having a primary temperature characteristic and, wherein the constant voltage generated is substantially independent of the number of the plurality of first bipolar transistors and the number of the plurality of second bipolar transistors.

The present invention also provides a constant voltage generating circuit comprising a plurality of first npn transistors including n (an integer; $2 \leq n$) first npn transistors, a base and a collector of each of the plurality of first npn transistors being connected together, an emitter of a one of the plurality of first npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first npn transistors being connected to a collector of a (k-1)-th one of the plurality of first npn transistors, a plurality of second npn transistors including n second npn transistors each having an emitter area greater than each of the plurality of the first npn transistor, a base and a collector of each of the plurality of second npn transistors being connected together, an emitter of a one of the plurality of second npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of second npn transistors being connected to a collector of a (k-1)-th of the plurality of second npn transistors, a current source connected to the collector of a n-th one of the group of plurality of first npn transistors to supply a current to each of the pluralities of first and second npn transistors, two resistors being connected in series between the current source and a n-th one of the plurality of second npn transistors, and current control means comprising a first input terminal including a differential amplifier in which an offset voltage in input equivalent has a primary temperature characteristic, the n-th one of the plurality of first npn transistors being connected to the first input terminal, and a second input terminal

to which a connection point between the two resistors connected in series is connected, the current control means controlling a current from the current source by outputting a control signal that controls the current from the current source so that a potential at the first input terminal and a potential at the second input terminal are the same and, wherein the constant voltage generated is substantially independent of the number of the plurality of first bipolar transistors and the number of the plurality of second bipolar transistors.

The present invention also provides a constant voltage generating circuit further comprising a differential voltage generating means including a differential amplifier, and a offset voltage at the differential amplifier in input equivalent has a primary temperature characteristic, wherein the differential amplifier has a differential pair including a first npn transistor and a second npn transistor having a larger emitter area than the first npn transistor, and a first and second current sources to supply a first and second current to the differential pair, wherein the differential pair includes a first and second input terminals, the first input terminal is a base of the first npn transistor, and the second input terminal is a base of the second npn transistor, and wherein an emitter of the first npn transistor is connected to the first current source, and an emitter of the second npn transistor is connected to the second current source, the emitter of the first npn transistor being connected to the emitter of the second npn transistor.

The present invention also provides a constant voltage generating circuit further comprising a differential amplifier having a differential pair including a first npn transistor and a second npn transistor having a larger emitter area than the first npn transistor, and another current source that supplies a current to the differential pair, wherein the

differential pair includes a first and second input terminals, the first input terminal is a base of the first npn transistor, and the second input terminal is a base of the second npn transistor, and wherein an emitter of the first npn transistor is connected to the another current source, and an emitter of the second npn transistor is connected to the another current source, the emitter of the first npn transistor being connected to the emitter of the second npn transistor.

The present invention also provides a constant voltage generating circuit, wherein the differential amplifier has a differential pair including a first npn transistor and a second npn transistor having a larger emitter area than the first npn transistor, a first and second current sources to supply a current to the differential pair, and the differential amplifier has a second plurality of first npn transistors including m (an integer; $1 \leq m$) first npn transistors, and a second plurality of second npn transistors including m second npn transistors each having an emitter area greater than the second plurality of m first npn transistor, wherein the differential pair includes a first and second input terminals, the first input terminal is a base of the first npn transistor, and the second input terminal is a base of the second npn transistor, and wherein an emitter of the first npn transistor is connected to the current source, and an emitter of the second npn transistor is connected to the current source, the emitter of the first npn transistor being connected to the emitter of the second npn transistor, wherein a base and a collector of each of the pluralities of first npn transistors are connected together, a collector of k (an integer; $2 \leq k \leq m$)-th one of the second plurality of first npn transistor is connected to an emitter of a (k-1)-th one of the second plurality of first npn transistors, the collector of a one of the second plurality of first npn transistors is connected to the

emitter of the first npn transistor constituting the differential pair, and the emitter of an m-th one of the second plurality of first npn transistors is connected to the first current source, and wherein a base and a collector of each of the pluralities of second npn transistors are connected together, a collector of a k (an integer; $2 \leq k \leq m$)-th one of the second plurality of second npn transistor is connected to an emitter of a (k-1)-th one of the second plurality of second npn transistors, the collector of a one of the second plurality of second npn transistors is connected to the emitter of the second npn transistor constituting the differential pair, and the emitter of an m-th one of the second plurality of second npn transistors is connected to the second current source.